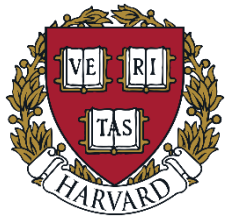
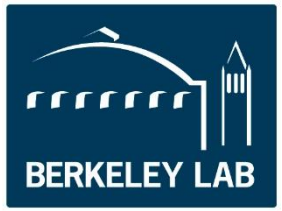
The Q-Pix pixelated readout concept for future LAr Time Projection Chambers: status and prospects

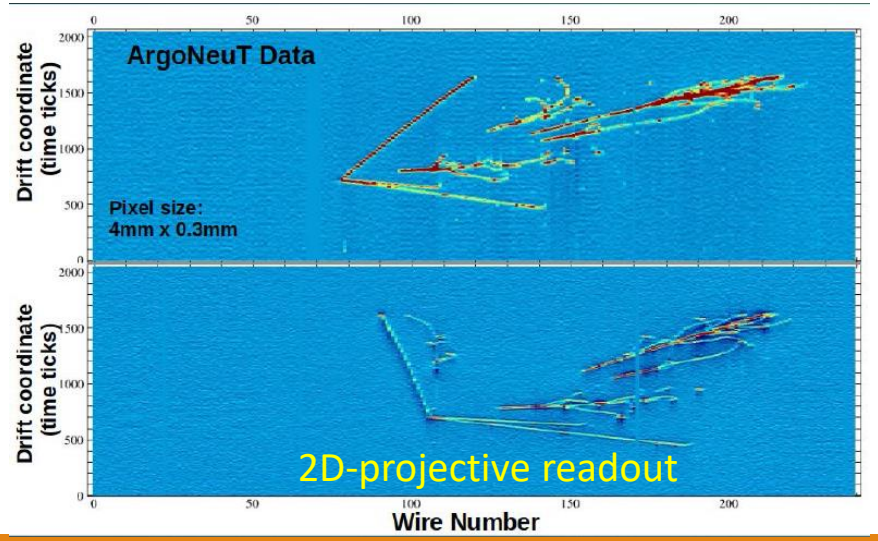
Gang Liu on behalf of the Q-Pix collaboration

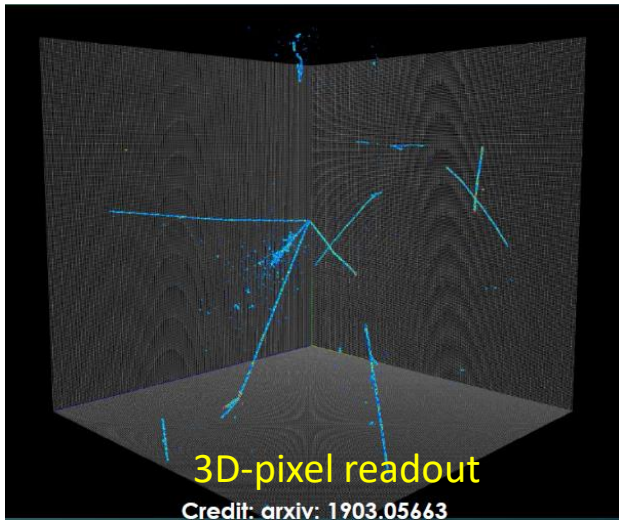





Introduction

- Liquid Argon Time Projection Chambers (LArTPC's) offer access to very high quality and detailed information
- Leveraging this information allows unprecedented access to detailed neutrino interaction specifics from MeV – GeV scales
- Capturing this data w/o compromise and maintaining the intrinsic 3-D quality is an essential component of all LArTPC readout





LAr pixel readout vs. wire readout

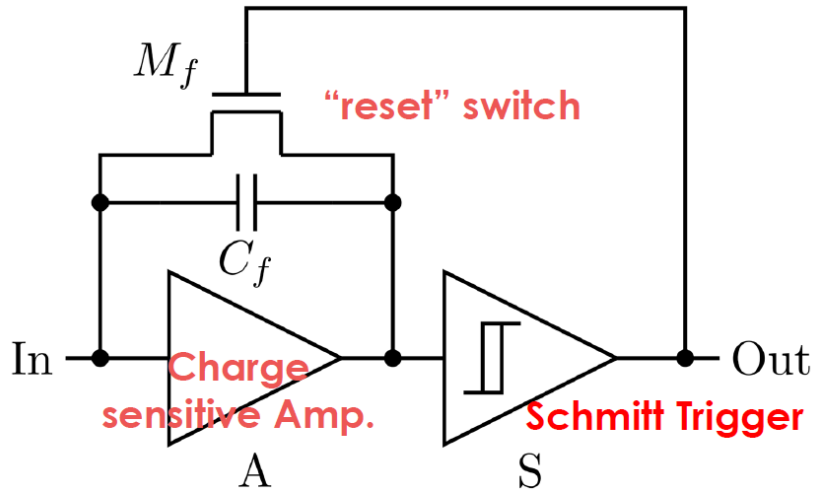
- Conventional LArTPC's use sets of wire planes at different orientations for reconstruction
  - Challenge in reconstruction of complex topologies
- Kiloton scale LArTPC's use 'wrapped wire' geometries to reduce the number of channels
  - Challenge to engineer such massive structures
- Being able to readout using pixels instead of wires could be a solution
  - Cost much more channels!
  - Example: 2 meter x 2 meter readout : **3mm wire pitch w/ three planes = 2450 channels**

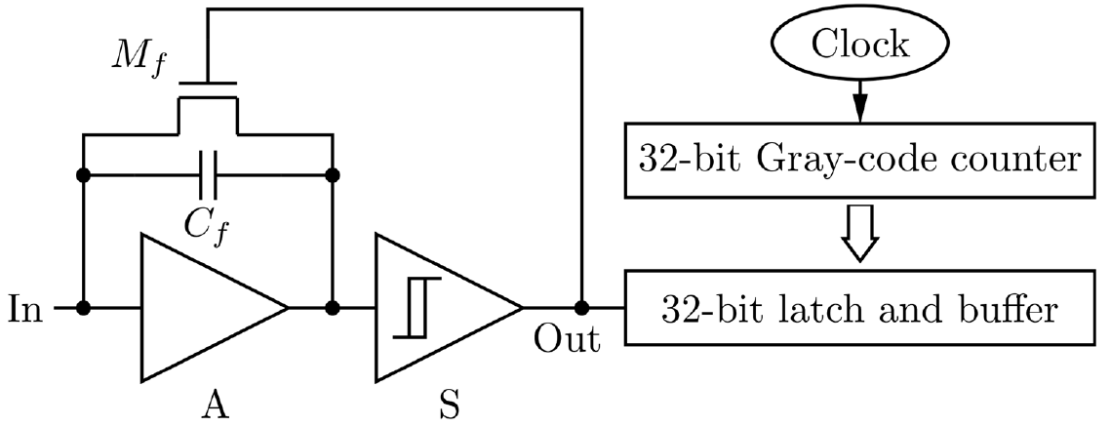
    3mm pixel pitch = 422,000 channels
- Pixel solution requires innovation in the readout electronics
  - Need to meet the heat load restrictions w/ a 100X higher channel number
- Requires an 'unorthodox' solution

‘unorthodox’ solution

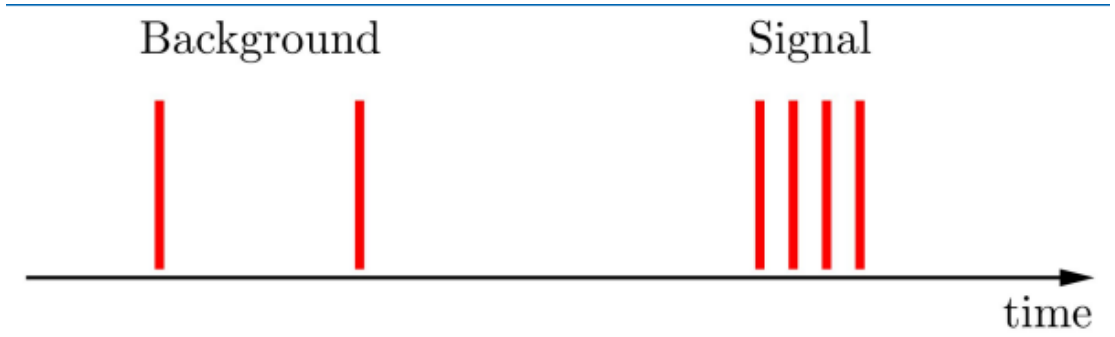
- Kiloton scale LArTPC’s (such as DUNE) afford a huge ‘big data’ challenge
- Most of the time there is ‘nothing of interest’ , but must be ready when something happens
- The Q-Pix pixel readout follows the ‘electronic principle of least action’
  - **Don’t do anything unless there is something to do**
    - Offers a solution to the immense data rates
    - Allows for the pixelization of massive detectors
- Q-Pix offers an innovation in signal capture with a new approach and measure **time-to-charge**
  - Preserves the detailed waveforms of the LArTPC
  - Attempts to exploit 39Ar to provide an automatic charge calibration

Q-Pix: the Charge Integrate-Reset (CIR) Block



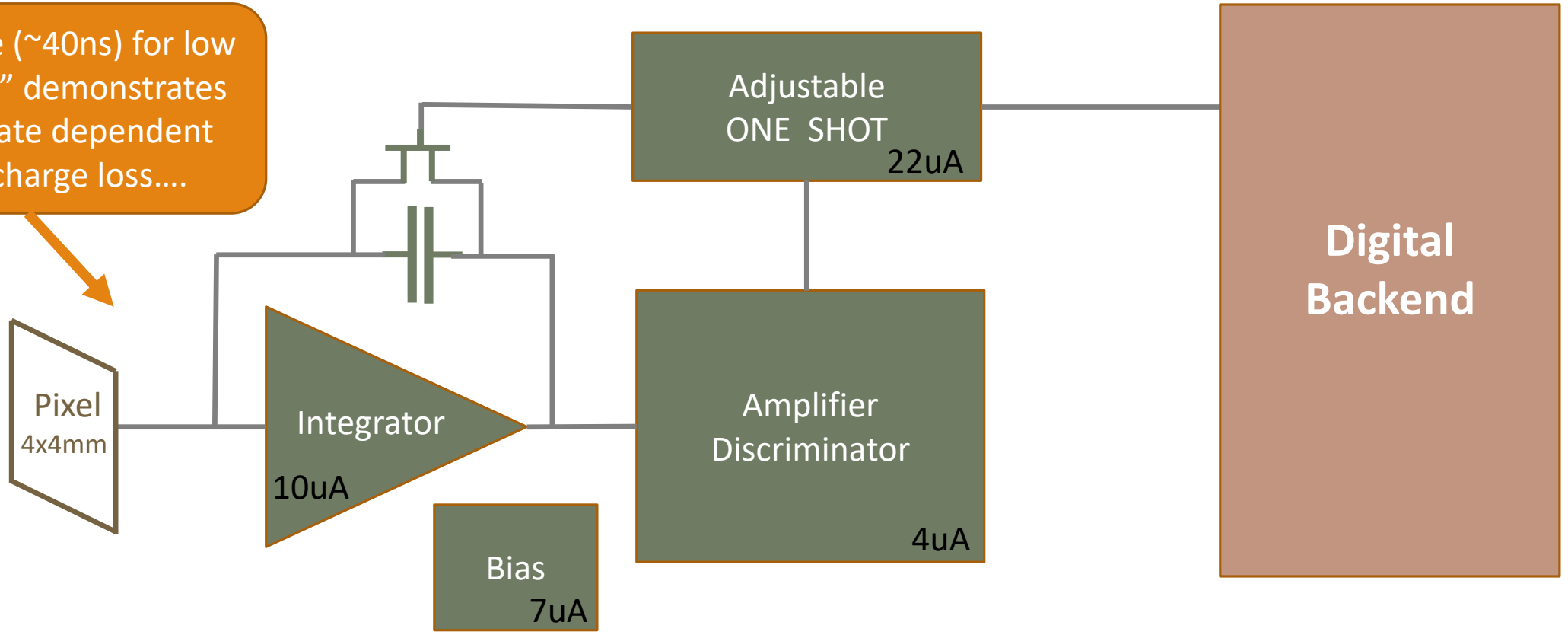


- Charge from a pixel (In) integrates on a Charge sensitive amplifier (A) until a threshold is met which fires the Schmitt Triger (S) to cause a rest and the loop repeats
- Measure the time of the 'reset' with a local clock
- **R**eset **T**ime **D**ifference = ΔQ



Q-Pix analog front end - First attempt

The finite time (~40ns) for low power "reset" demonstrates instigates a rate dependent ionization charge loss….

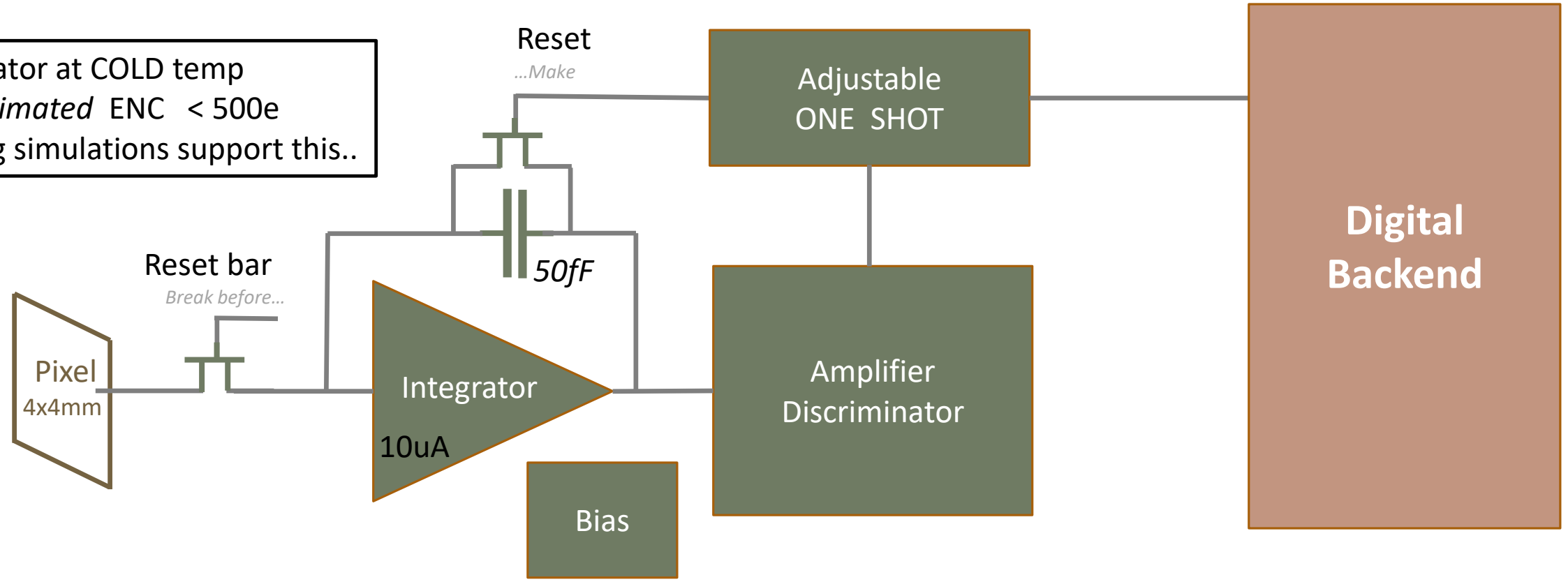


Schematic Level design in 180nm Silicon
Proven @LAr temperatures -186C°
re: LArASIC (BNL) and LArPix (LBNL)

Single (FE only) Channel POWER/ch	
Present FE Design	34µW
Projected final prototype FE	**25µW**

Q-Pix analog front end - Improved design

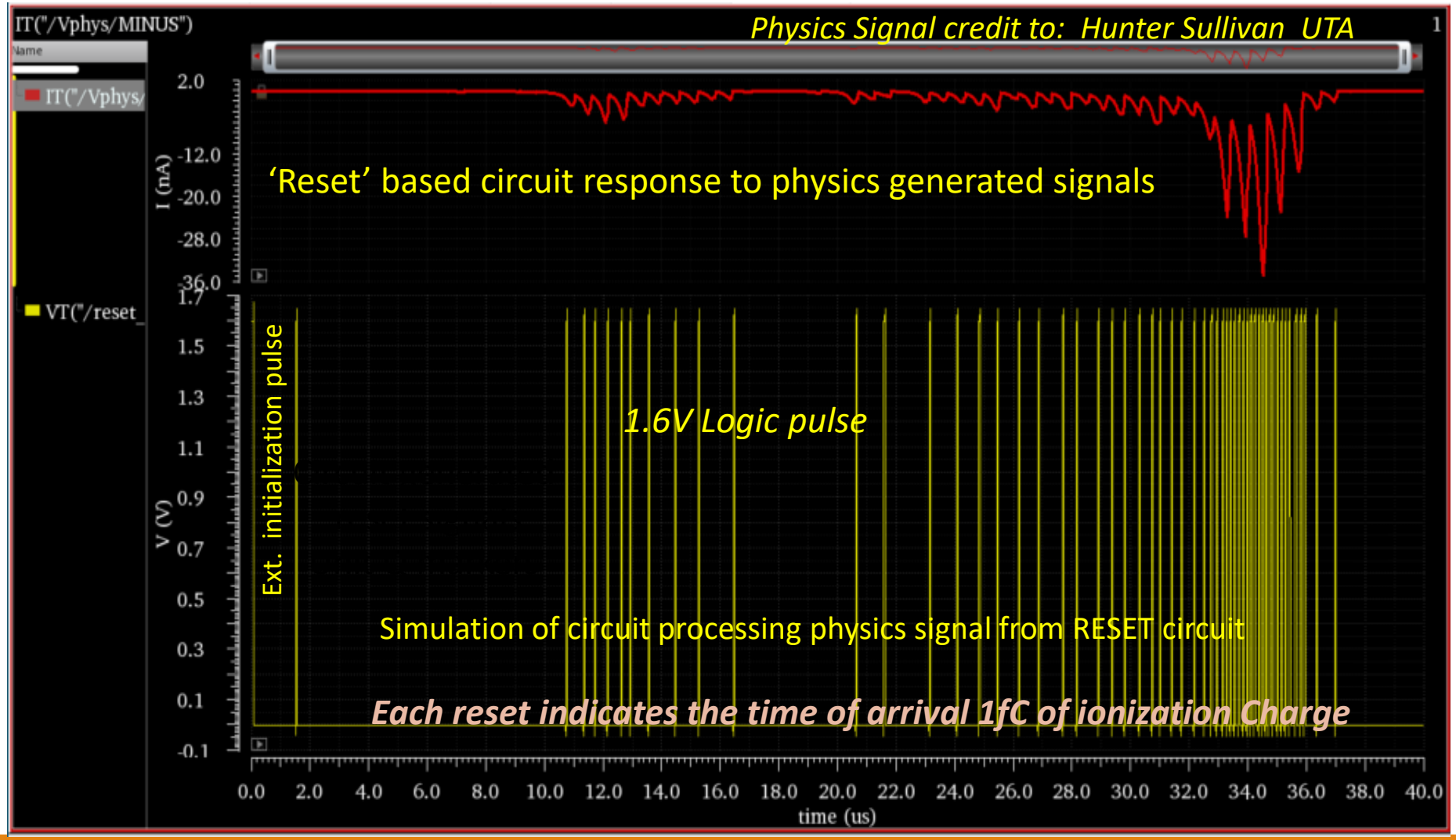
Integrator at COLD temp
…*estimated* ENC < 500e
Analog simulations support this..



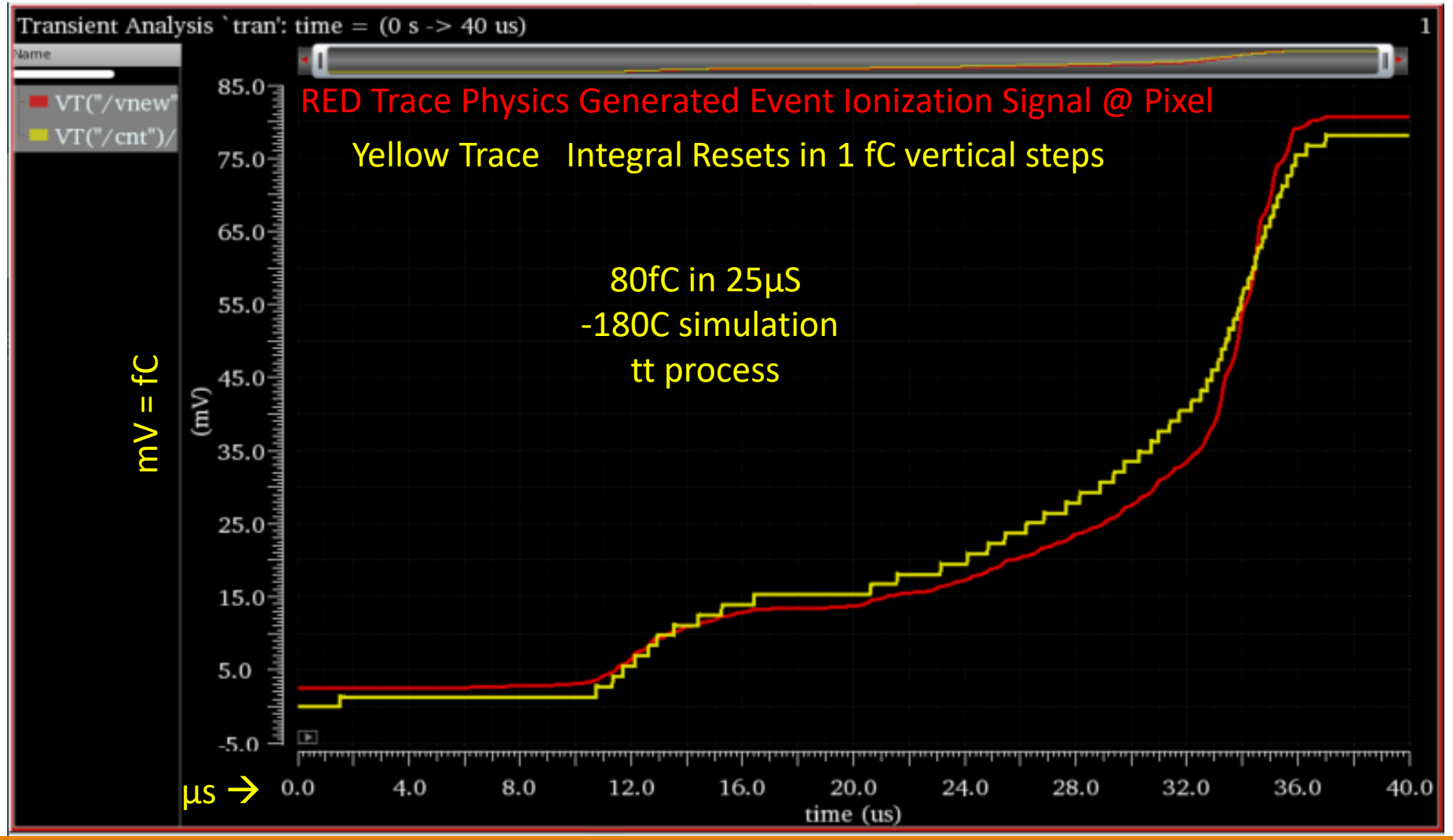
Schematic level 180nm Technology

Similar Power to Original

Simulation results with physics generated signal



Reconstruction of the signal using reset time marking



Fixed Q reset time marking circuit first pass assessment

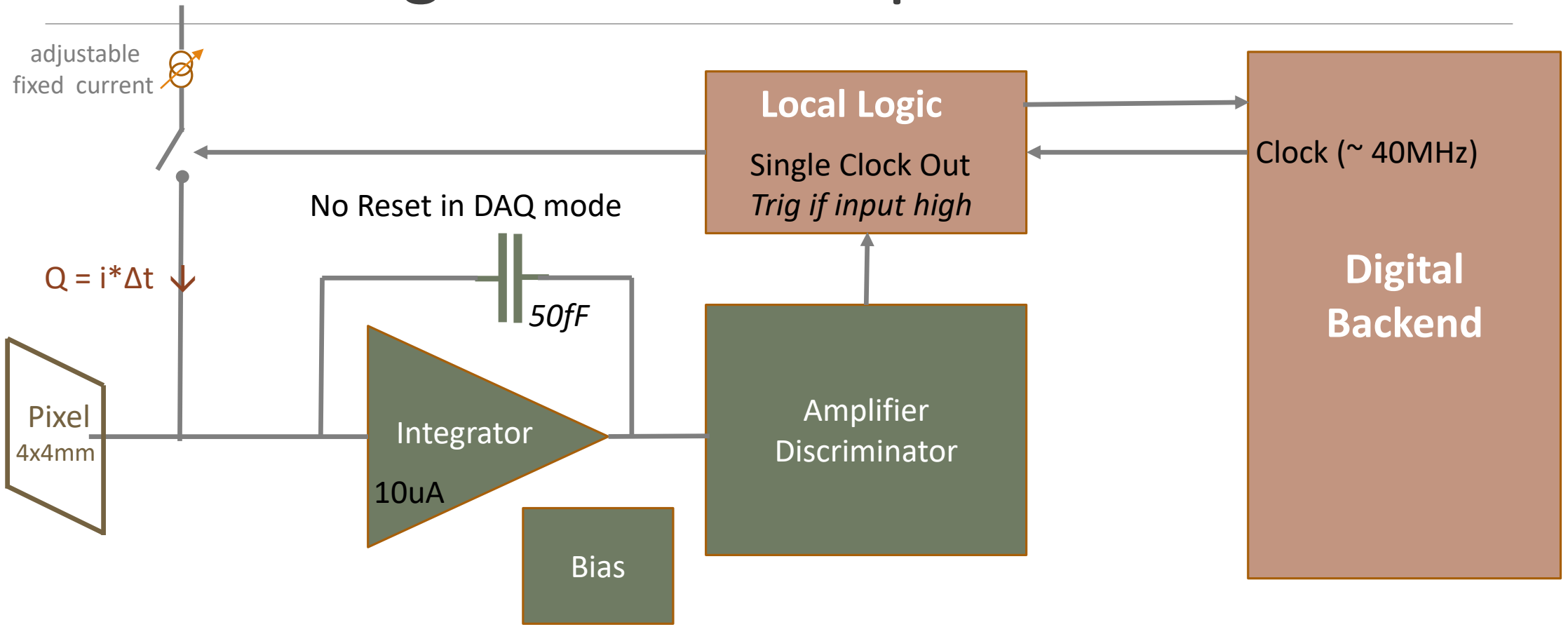
- Simple and reasonable approach
- Pixel accumulates charge causing “lag” that is not reset in time but charge loss is limited.
- Suitable for a prototype circuit (with some improvement)

- ***This version instigates a second idea:***

Why not simply replace the charge

… no need to disconnect from the pixel

Q-Pix analog front end - Replenishment circuit

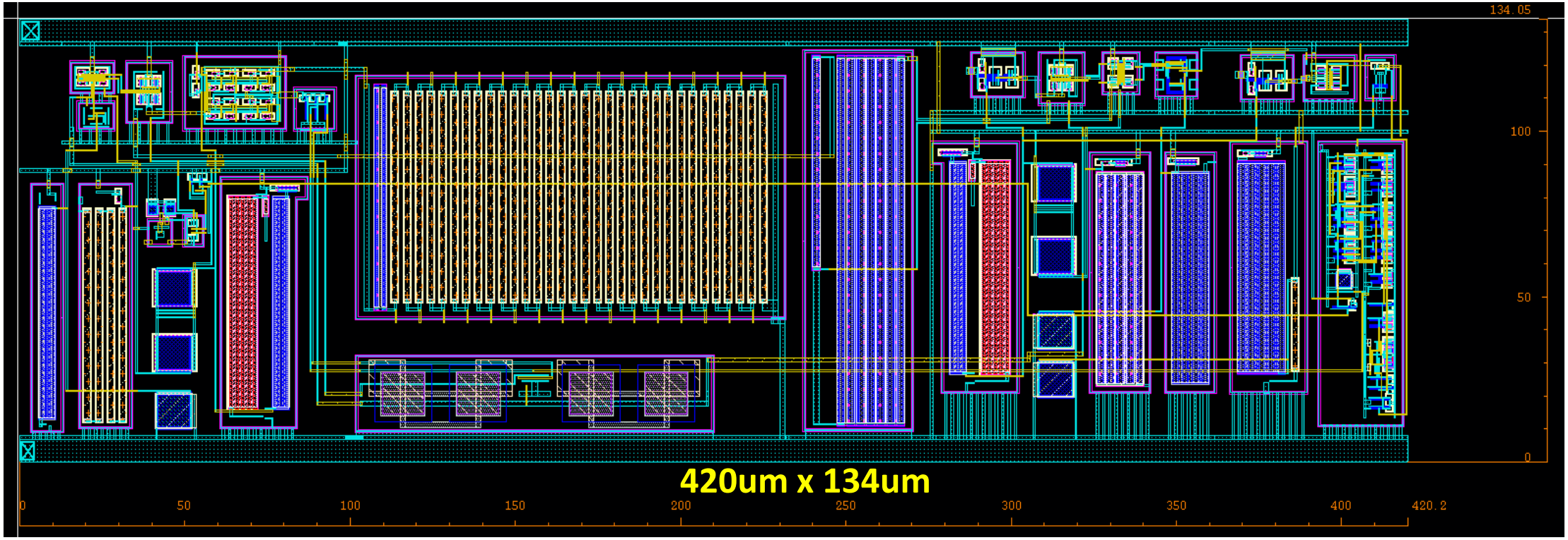


Schematic level 180nm Technology

Similar Power to Original

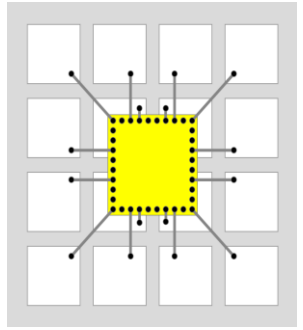
Full Replenishment Channel layout

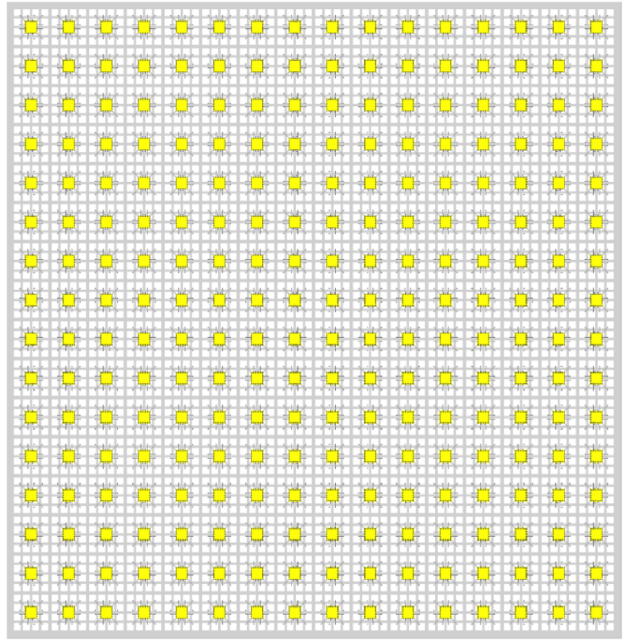
~ 40uW still to be optimized



Q-Pix digital back end concept

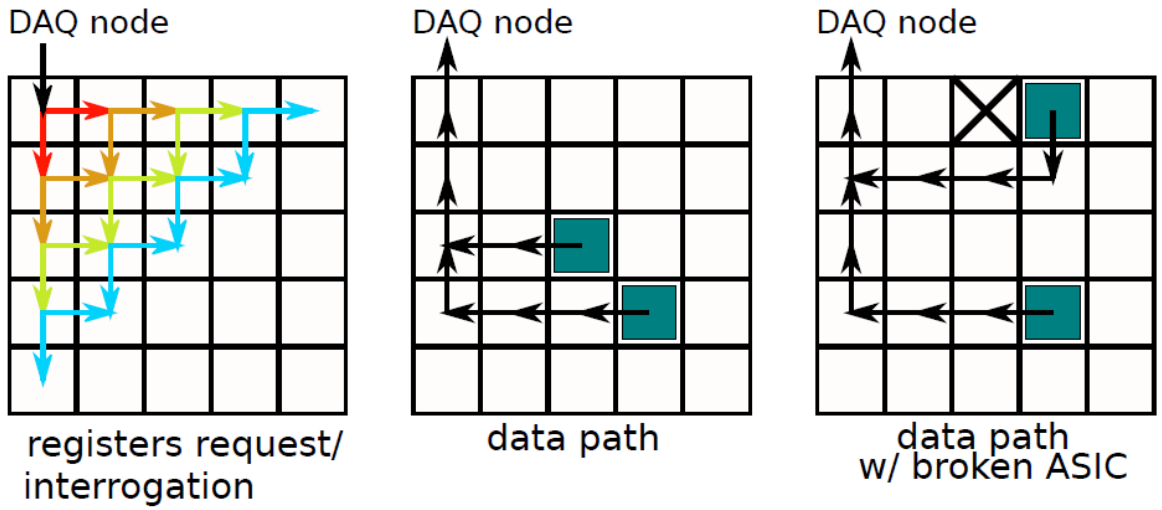
- 16 - 32 - 64 pixels / ASIC
  - 1 free-running clock/ASIC
  - 1 capture register for clock value
  - Necessary buffer depth for beam/burst events
  - State machine to manage dynamic network, token passing, clock domain Crossing, data transfer to network
- Basic unit would be a ‘tile’ of 16x16 ASICs (4096 4mm x 4mm pixels)
  - Tile size 25.6cm x 25.6cm

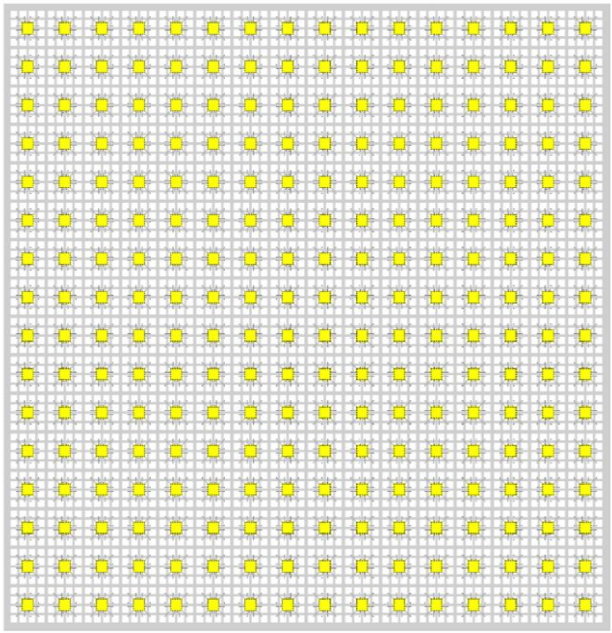




Q-Pix operating principle – programmable-data-path network

- Q-Pix ASICs: **programmable-data-path** network and **asynchronous** communication
  - **programmable-data-path**: The readout data path could be programmable to build up the network through one another.
    - This network should be robust, no single failure should make the tile unusable.
    - Only one or a few ASICs talk to the outside world to simplify the overall system.
    - Register R/W (including trigger) is broadcasted to all neighbor ASICs.
    - If ASIC coordinates are specified then only given ASIC preforms the action.



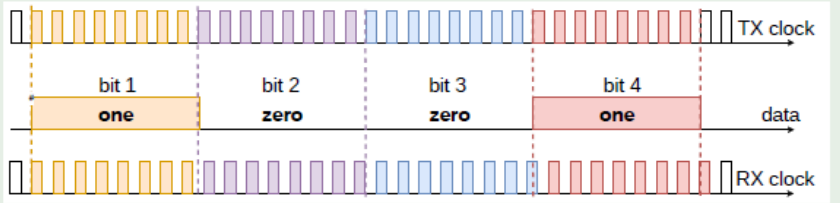


Q-Pix operating principle – asynchronous communication

- Q-Pix ASICs: **programmable-data-path** network and **asynchronous** communication
  - **Asynchronous**: each ASIC runs on its own clock at a given nominal frequency.
    - Clock frequency may differ slightly.
    - Asynchronous communication protocol should be able to tolerate the frequency difference.
    - Two protocols have been implemented so far

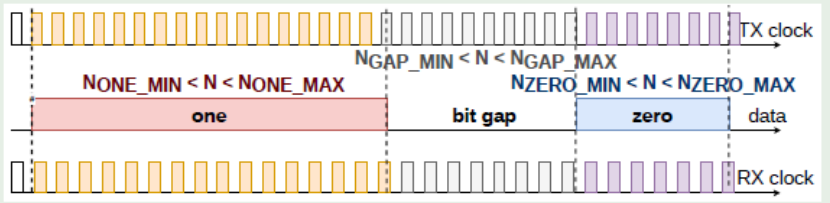
UART

- Atomic by word
- Tolerance depends on the word length, and about 1.5% for 64-bit word.



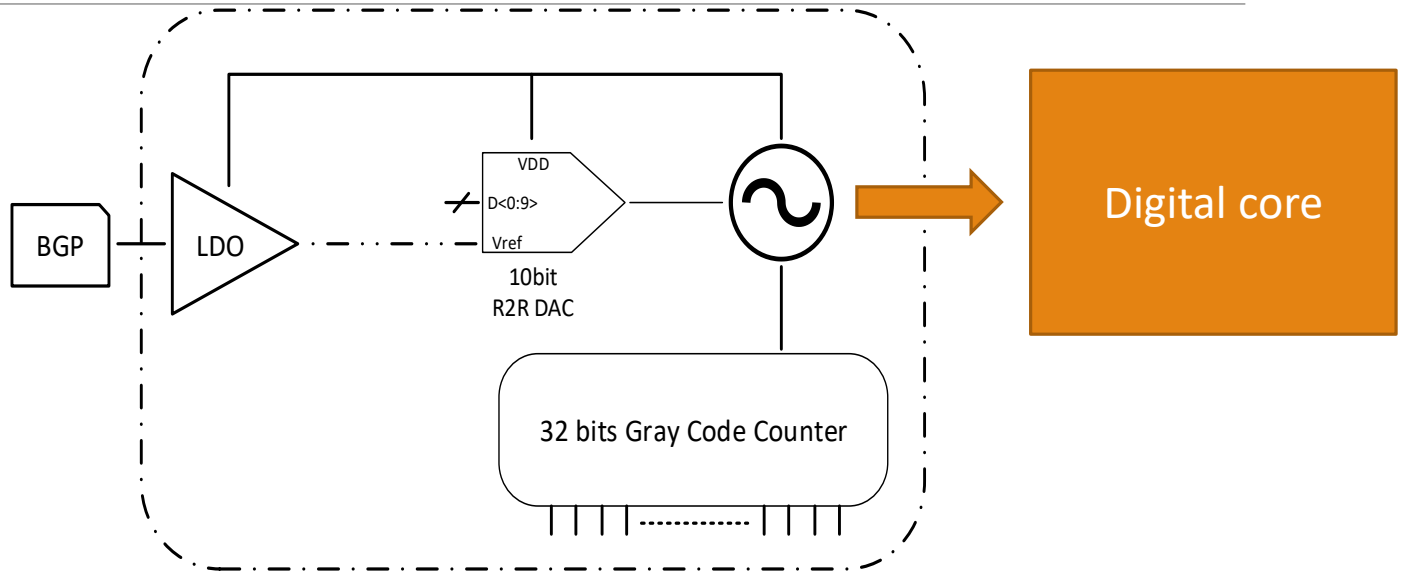
"Endeavor"

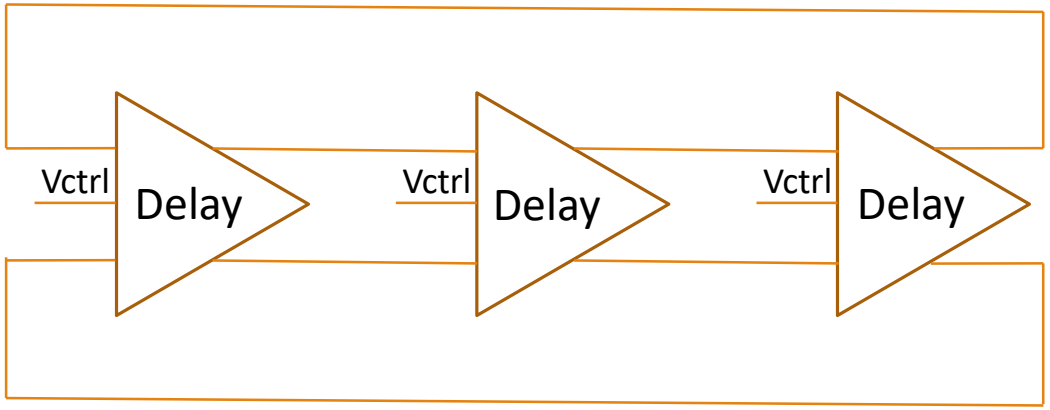
- Morse code approach, atomic by bit
- Tolerance to the difference in clock frequencies increases with the decreasing the bit rate.

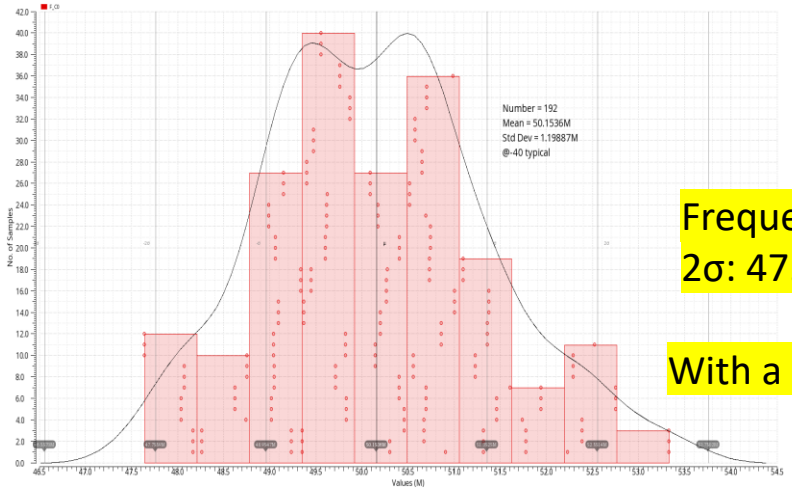


Free running clock

- 3 stage ring oscillator
- Differential structure
- R2R DAC and power supply component

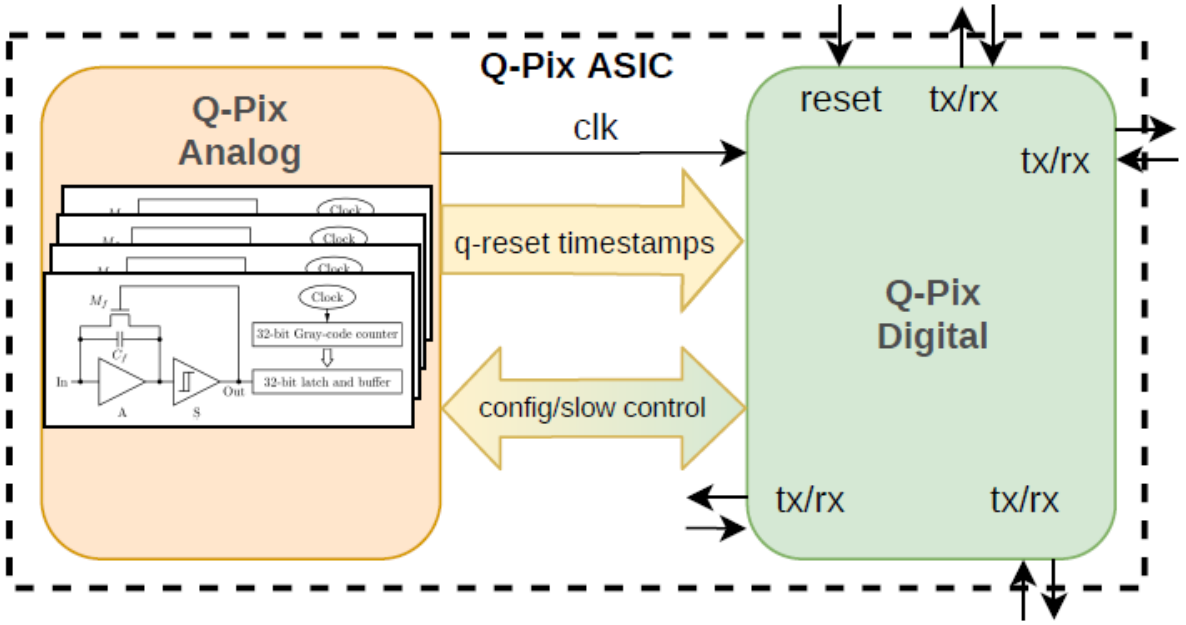






Frequency monte carlo simulation
2σ: 47.76M ~52.56M @-40 typical
Approx +/- 4.5%
With a power of 0.35mW @ 50MHz

Q-Pix digital prototype plan

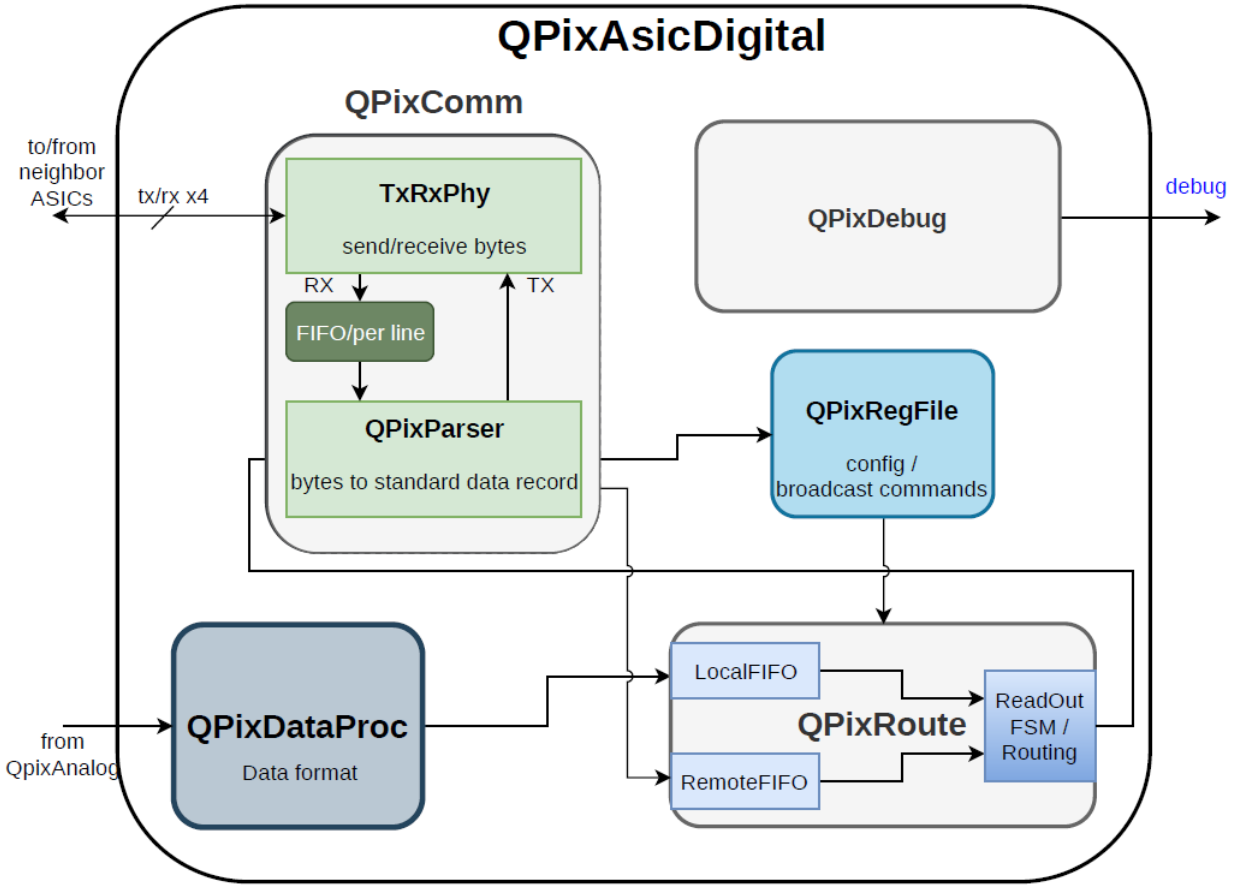


Options

1. A single chip comprising both analog and digital components
2. Two separate chips. Q-reset pulses are being fed to digital component instead of timestamps.

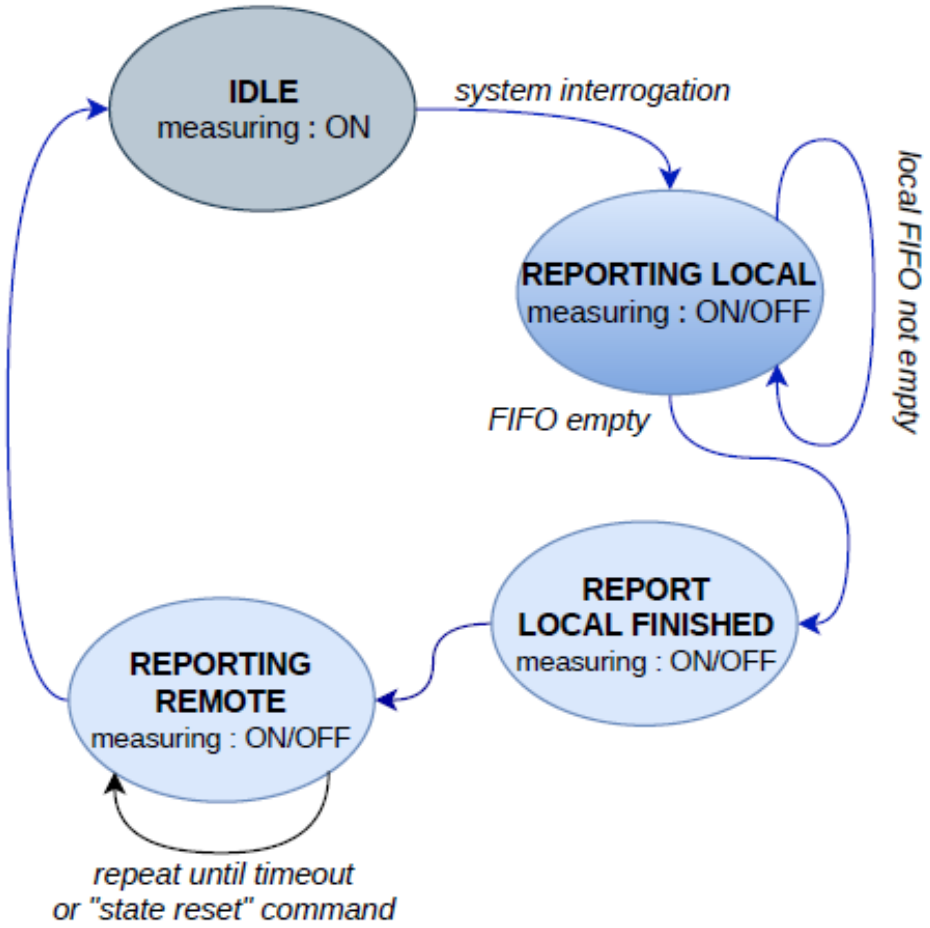
- Goals
  - Receive and buffer the timestamps of the charge reset signal from the analog part.
  - Combine data packets containing the timestamps, channel number along w/ the service information like error flags.
  - Route the data packets from the ASICs where they are generated to DAQ node.

Q-Pix digital back end structure

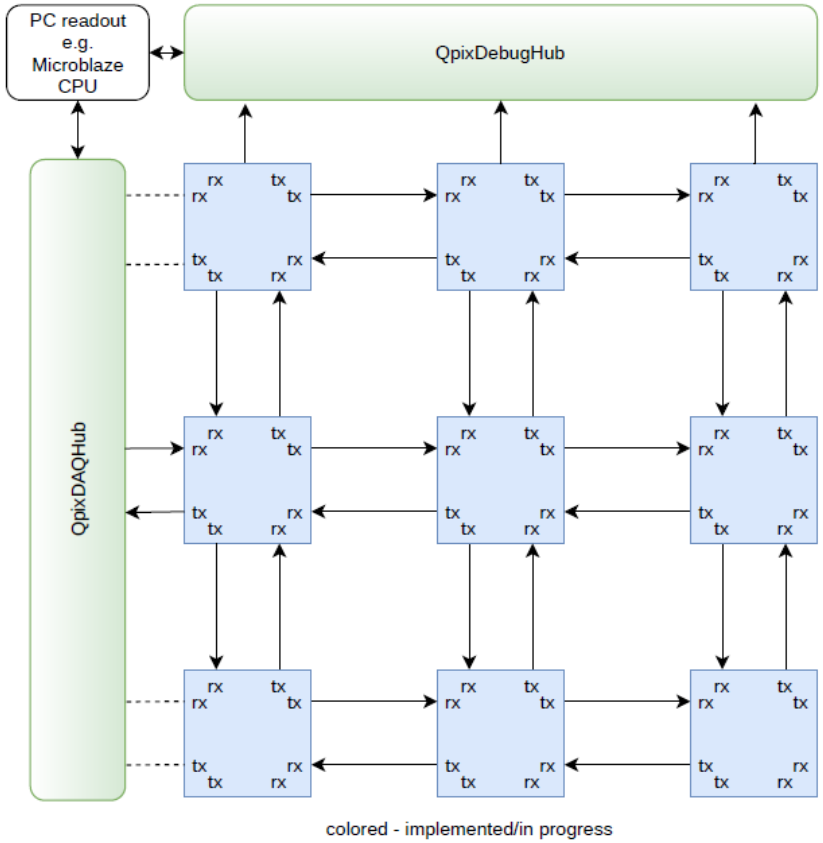


- QPixComm: communication with other ASICs
- QPixRegFile: store the configuration and status
- QPixDataProc: receive the data from analog part
- QPixRoute: contain FIFO for local and remote hits, also contain routing FSM
- QPixDebug: for debugging

Basic state machine scheme

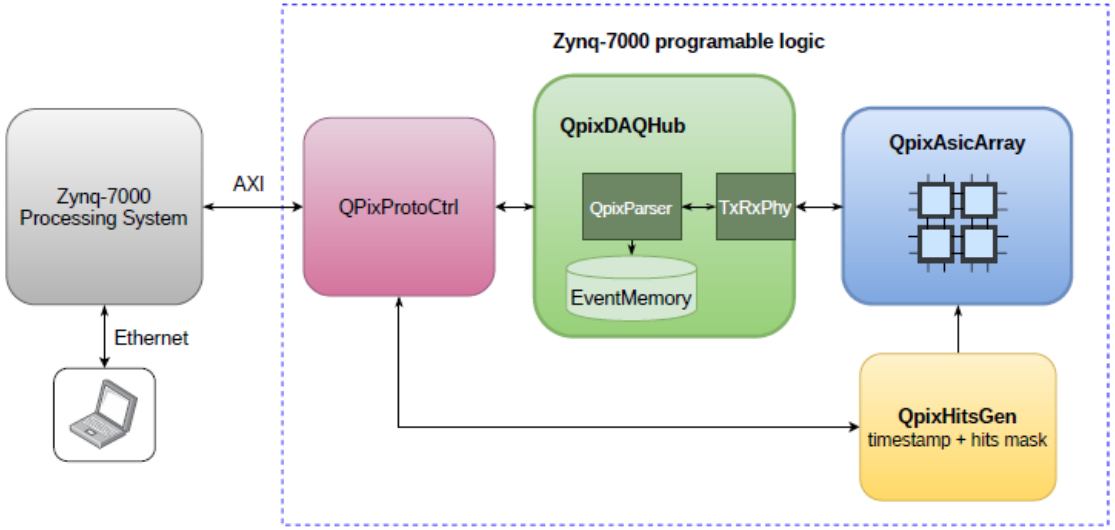


Q-Pix digital prototyping and verification



colored - implemented/in progress

ASICs with 4 connections are being used as the most generic example. In future we will study different connection schemes.



Device

- Xilinx Zynq-7000 SoC
- Readout through ARM processing system
- Communication with PC via 1G Ethernet

Prototyping goals

- Implement the full functionality of the chips
- Test and optimize : routing schemes, chips connectivity, data formats, register mapping etc.
- Template for a DAQ module firmware as a byproduct

Summary and Outlook

- Low power pixel based readout for LArTPC's have promise to enhance the capabilities of these detectors
  - The LArPix team has pioneered the demonstration of this technology for application to the DUNE detector
  - Q-Pix is futuring this work to target the low occupancy environment found in the DUNE far detector
- Three versions of the low power Front-end circuit have been developed
- A back-end readout method based on the programmable-data-path network and asynchronous communication has been implemented
- The prototype ASIC in under development, which will answer many important questions
- Q-Pix consortium would like to thank the DOE for its support

Thanks !